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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/880,404 | 06/12/2001 | Akila Sadhasivan | 42390P10595 | 7126 |

7590 09/02/2003

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| EXAMINER |
|---|
| TAKEGUCHI, KATHY K |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2187 | |

DATE MAILED: 09/02/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/880,404 | Applicant(s) SADHASIVAN ET AL. | |
|---|---|---|---|
| | Examiner Kathy Takeguchi | Art Unit 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14,19-21 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,19-21 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. The present Office Action is a Non-Final Action taken in response to examination of Claims 1-14, 19-21, and 25-29, presented in the instant application. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56.

### *Claim Objections*

2. Claim 8 is objected to because of the following informalities:

In Claim 8 (line3), "performed on a memory device" should be changed to "performed on the memory device" to properly refer back to "a memory device", which is in line 2.

In Claim 8 (line 4), --memory-- should be inserted before device.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5-7, and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Hazen et al (United States Patent 6,088,264).

As per Claims 1 and 6-7:

Hazen teaches a method of performing multiple operations on a memory device, comprising:

- dividing the memory device (e.g., "the flash memory device"; EEPROM) into k partitions (e.g., Figure 2, Figure 3), wherein k is an integer greater than or equal to two (e.g., Column 3, lines 39-40: "The number of partitions depends upon the function of the flash memory"; Figure 2 illustrates n partitions, whereas Figure 3 illustrates a three partitioned flash memory);
- performing code operations from m code partitions out of k total partitions, wherein m is an integer greater than or equal to one (e.g., Column 3, lines 55-59); and
- performing data operations from n data partitions out of k total partitions through low level functions accessed from the code partitions at *approximately* the same time as the code operations are performed from the m code partitions, wherein n is an integer

greater than or equal to one (e.g., Column 3, lines 55-59: "Another example of a three partitioned flash memory device is having *code executed from a first partition, while updating data in a second partition.* Thus, for example, if the code execution results in an updating of the data, this can be accomplished seamlessly").

As per Claims 2 and 5:

Hazen further teaches a method, wherein the data partitions and code partitions do not overlap each other in the memory device and are fixed in memory space (e.g., Figure 2; Figure 3; Column 2, lines 26-29: "Each partition is implemented as a physically separate device on the flash memory device. For one embodiment, each partition is implemented on a different physical plane.").

As per Claim 3:

Hazen further teaches a method, wherein the m code partitions and the n data partitions equal the k total partitions (e.g., Column 3, lines 44-54: "One example of using a three partitioned flash memory device is as follows. A first partition may be used to store data. A second partition may be used to store code, that is executed by an apparatus that includes the flash memory device. The third partition may be used to permit updating of code. Thus, for example, if the code changes as a result of an update, new code is written to the third partition while the original code in the second partition is currently executing. When the new code has been written and verified, the third partition can become the partition used for the code." Three Partitions = Partition#1(Data) + Partition#2(Code) + Partition#3(Code); Column 3, lines 39-41).

As per Claims 11 and 14:

Hazen teaches a flash memory array, comprising:

- a plurality of partitions (e.g., Figures 2 and 3);
- a status mode to provide partition status from the memory device (e.g., Column 2, lines 60-64);
- a read mode to read code and data from the memory device (e.g., read operation); and
- a write mode to write data to the memory device (e.g., write operation).

As per Claim 12:

Hazen teaches a memory array, wherein the code is programmed into the memory array (e.g., Column 3, lines 39-59).

As per Claim 13:

Hazen teaches a memory array, wherein the write mode is also capable of performing erase operations on data stored in the memory array (e.g., Column 3, lines 13-19).

5. Claims 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Brown et al (United States Patent 6,201,739).

As per Claim 19:

Brown teaches a memory device with k partitions (e.g., code and data partitions, Figure 10), wherein k is an integer greater than or equal to two; low level functions to access the memory device (e.g., Figure 9); and a flag to indicate when a suspend operation has occurred (e.g., suspend signal in Figures 10 and 11).

As per Claims 20-21:

Brown et al teach a flash memory device comprising at least one code partition and at least one data partition (e.g., code partition and data partition, Figure 10).

6. Claims 8-10 and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hansen et al (United States Patent 5,822,244).

As per Claim 8:

Hansen teaches an apparatus comprising:

- means for partitioning a memory device (e.g., Figure 3: flash memory (12) includes two partitions = memory array (20) and memory array (22)) to enable multiple operations to be performed on the memory device at the same time (e.g., RWW operation: Column 3, line 65 to Column 4, line 4); and

- means for tracking operations performed on the memory device to restore interrupted tasks (e.g., status registers and control signals allow for resuming the interrupted program/erase operation).

As per Claims 9 and 10:

Hansen teaches an apparatus capable of saving and suspending a program/erase operation so that a read operation can occur and later resuming the program/erase operation (e.g., Figure 4).

As per Claim 25:

Hansen teaches a method, comprising:

- running a first operation on a first partition of a memory array (e.g., Column 3, line 65-67);
- running a first operation on a second partition of a memory array (e.g., Column 3, line 65-67);
- requesting a second operation to be performed on the first partition (e.g., request a read operation); and
- determining if the second operation has a higher priority than the first operation (e.g., Figure 4).

As per Claims 26 and 28:

Hansen further teaches suspending the first operation if the second operation has a higher priority than the first operation and running the second operation in the first partition (e.g., Figure 4: program/erase suspended because read operation has priority if the first operation in the first partition is a program/erase operation and the second operation is a read operation).

As per Claim 27:

Hansen further teaches setting a flag to indicate that the first operation must resume after the second operation is completed (e.g., suspend/resume control).

As per Claim 29:

Hansen further teaches suspending the first operation if the second operation has a higher priority than the first operation (e.g., Figure 4: program/erase command is ignored because the read operation has priority if the first operation in the first partition is a read operation and the second operation is a program/erase operation).

## *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hazen et al (United States Patent 6,088,264) in view of Lee (United States Patent 6,377,486).

As per Claim 4:

Hazen teaches a method of claim 1, but does not specifically teach that each of the m code partitions are equal in size to each of the n data partitions.

However, Lee teaches the concept of having a flash memory with each of the m code partitions being equal in size to each of the n data partitions (e.g., Figures 1 and 3).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Hansen for the added benefit of uniformity and being able to provide the same system requirements/needs for each partition.

***Response to Arguments***

9. The applicants' arguments are moot in view of the new ground(s) of rejection.

However, the following argument is still applicable and is addressed below:

- **Applicants' Argument**: "The Examiner states that Brown teaches a memory device with k partitions in figure 10. (3/1/03 office action, page 4). Applicants respectfully disagree. Figure 10 of Brown simply shows a flash EPROM that stores both code and data. (Brown, column 9, line 49). The flash EPROM of Brown does not have k partitions as set forth in Claim 19."
- **Response:** The applicants' arguments are not persuasive because Brown does teach a memory device with k partitions. Figure 10 clearly illustrates a flash EPROM in which the code is partitioned separately from the data. Furthermore, as noted by the applicants, Brown does state that in Figure 10 "the flash EPROM stores both code and data". Brown also teaches that in certain flash EPROMs, "code is stored in certain blocks of the flash EPROM, and data is stored in other blocks of the flash EPROM" (e.g., Column 3, lines 35-38). Thus, Brown teaches a flash EPROM with k partitions (e.g., interpreted as partitions = blocks; interpreted as partitions = portion containing code + portion containing data).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kathy Takeguchi whose telephone number is (703) 305-8115. The examiner can normally be reached on Monday - Friday, 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

KT
Kathy Takeguchi
Art Unit 2187
August 25, 2003

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100